Influence of ceramic package internal components on the performance of vacuum sealed uncooled bolometric detectors

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ABSTRACT

INO has developed a hermetic vacuum packaging technology for uncooled bolometric detectors based on ceramic leadless chip carriers (LCC). Cavity pressures less than 3 mTorr are obtained. Processes are performed in a state-of-the art semi-automated vacuum furnace that allows for independent activation of non-evaporable thin film getters. The getter activation temperature is limited by both the anti-reflection coated silicon or germanium window and the MEMS device built on CMOS circuits. Temperature profiles used to achieve getter activation and vacuum sealing were optimized to meet lifetime and reliability requirements of packaged devices. Internal package components were carefully selected with respect to their outgassing behavior so that a good vacuum performance was obtained.

In this paper, INO's packaging process is described. The influence of various package internal components, in particular the CMOS circuits, on vacuum performance is presented. The package cavity pressure was monitored using INO's pressure microsensors and the gas composition was determined by internal vapor analysis. Lifetime was derived from accelerated testing after storage of packaged detectors at various temperatures from room temperature to 120°C. A hermeticity yield over 80% was obtained for batches of twelve devices packaged simultaneously. Packaged FPAs submitted to standard MIL-STD-810 reliability testing (vibration, shock and temperature cycling) exhibited no change in IR response. Results show that vacuum performance strongly depends on CMOS circuit chips. Detectors packaged using a thin film getter show no change in cavity pressure after storage for more than 30 days at 120°C. Moreover, INO's vacuum sealing process is such that even without a thin film getter, a base pressure of less than 10 mTorr is obtained and no pressure change is observed after 40 days at 85°C.

Keywords: hermetic vacuum packaging, bolometers, MEMS, non-evaporable getter.

1. INTRODUCTION

Uncooled bolometric detectors are among the MEMS devices that have the most stringent requirements for vacuum hermetic packaging.[1] Depending on bolometer geometry, the infrared responsivity starts to degrade at a pressure above a few mTorr. Over the years, INO has demonstrated a strong expertise in the fabrication of various types of uncooled bolometers and the hermetic vacuum packaging of these focal plane arrays (FPA).[2] The various packaging technologies developed include a metallic package with integrated thermoelectric cooler , TEC, and pump-out tube for high-end applications,[3] a ceramic package with integrated TEC and a vacuum port[2] and a hybrid wafer-level micropackaging technology.[4] In recent years, a number of wafer-level packaging approaches have been proposed to reduce packaging cost.[5] However, due to the cavity volume of a few microliters, major challenges have to be overcome to achieve the vacuum integrity required by most imaging applications. This paper presents some key aspects of package design and performance of a TECless ceramic leadless chip carrier (LCC) technology with a soldered window lid, thus featuring window assembly and vacuum sealing in a single step. It offers an alternative solution for low-cost, reduced footprint and high throughput production of uncooled focal plane arrays.

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Reliability, Packaging, Testing, and Characterization of MOEMS/MEMS and Nanodevices XII,
edited by Rajeshuni Ramesham, Herbert R. Shea, Proc. of SPIE Vol. 8614, 86140G
© 2013 SPIE · CCC code: 0277-786X/13/$18 · doi: 10.1117/12.2005945

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It is well known that a vacuum packaging technology based on a soldering process suffers from a high gas load level during the sealing step. Typical vacuum levels obtained after sealing are on the order of 1 Torr.[6,7] Thus, the use of a non evaporable getter technology is essential for pumping this gas load and extending the lifetime of the product.

An additional difficulty related to the soldering process comes from the temperature sensitive MEMS-MOEMS devices. Bolometer FPAs are fabricated over CMOS wafers that have a maximum process temperature to avoid damage to the circuitry. Solder alloys are usually preferred for die-attach due to reduced outgassing and enhanced thermo-mechanical properties as compared to polymers. However, some CMOS chips cannot withstand a typical soldering die attach, nor a window lid soldering, using the AuSn fluxless alloy having a reflow temperature above 300°C. In this paper, a die-attach process based on an organic material was investigated. Previous work showed that with proper choice of adhesive, cure process and getter materials, it is possible to obtain and maintain sealed devices with internal vacuum levels less than 20 mTorr.[8]

To monitor pressure levels in the package cavity, micro-Pirani pressure gauges developed at INO were used.[9] As compared to other leak rate measurement techniques such as conventional bombing methods, these microsensors have a better sensitivity. They can provide enough sensitivity to assess package hermeticity at leak rate levels of $7.5 * 10^{-16}$ Torr*L/s.[1] Another useful method for vacuum package analysis is the high resolution internal vapor analysis, HR-IVA.[10] This destructive method allows the identification of outgassed species and the determination of total pressure. These testing methods were used to determine the influence of internal components on the performance of vacuum sealed uncooled bolometers. Finally, the reliability, yield and lifetime estimation of the proposed packaging technology is presented.

2. DESCRIPTION OF INO'S LCC VACUUM PACKAGING TECHNOLOGY

2.1 General overview of package and process design

The development of a vacuum packaging technology requires a careful selection of each component with particular attention to their outgassing properties. The rationale for the choice of materials and process steps is described below. The header was a ceramic quad flat non-leaded package (Kyocera) with a die cavity of approximately 16 mm squared by 1.4 mm thick, an overall dimension of 24 mm squared and 68 electrical connections, Fig. 1. In order to accommodate different MEMS-MOEMS devices, the vacuum packaging technology presented in this paper may be applied to this generic family of ceramic packages by varying cavity size, footprint and pin number.

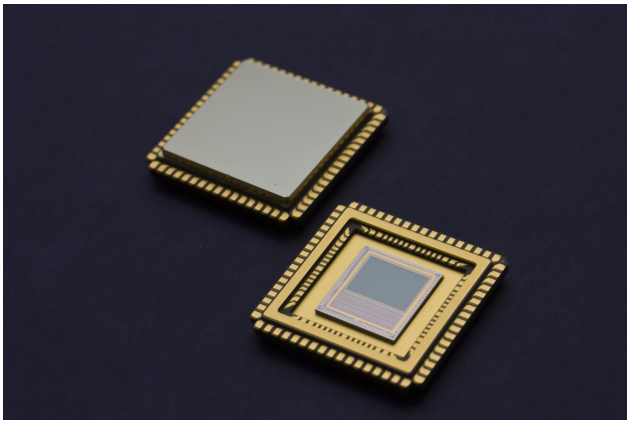

Figure 1. Photo of INOs ceramic 68LCC package equipped with a germanium window.

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The cleaning of parts is the first step to ensure that no contaminant gets in the cavity. Organic species must be removed prior to the assembly and vacuum sealing. The second step is the bake-out of components. The ceramic package itself is an important source of outgassing. Besides, electroplated nickel and gold layers present in metalizations trap significant amount of hydrogen. A proper bake-out consists of heating the parts at elevated temperature (250-400°C) in a high vacuum environment ($< 10^{-4}$ Torr). One limitation is the nickel diffusion into the gold layer at high temperature.[11] This phenomenon could possibly affect the soldering ability unless there is no contact to air after the process. The CMOS chip bake-out process must maintain reliability while being efficient in removing different entrapped gases. A trade-off between process time and temperature must be determined for each CMOS. The overall packaging process presented here employs a maximum temperature of 285°C.

The choice of die-attach adhesive is mainly driven by outgassing properties. The mass loss at the sealing temperature and the collected volatile condensable materials (CVCM) must be minimized and not exceed the ASTM E 595 low outgass specifications. The degradation temperature must be well above the highest process temperature. Table 1 summarizes parameters considered for choosing thermally conductive silicone and epoxy based adhesive materials that were used in this study.

Table 1. Relevant parameters specifications for organic adhesive tested for vacuum packaging.

Type	**Silicone**	**Epoxy**
Typical cure	30 min, 150 °C	60 min, 180 °C
% Mass loss	0.01%*	0.19%, 300 °C
% CVCM	0.004%	NA**
Degradation temp.	450 °C	330 °C

*Unknown temperature **Not available

Five packages with different adhesives were submitted to high resolution internal vapor analysis. The internal components and adhesive for each package sample are summarized in table 2. For the sake of comparison, the dispense amount of adhesives and the cure cycles were identical among packages. There is no getter and the chip attached is a fused silica chip, except for two packages where an FPA referred to as CMOS1 was present. The epoxy based adhesive yields higher base pressure as compared to the silicone based adhesive. The high base pressure level obtained is explained by the excess amount of adhesive dispensed so that the gas species partial pressure level could be measured. The results confirm that the nature of outgassed species strongly depends on the adhesive composition. The epoxy based adhesive mainly outgasses carbon dioxide (CO_2) while the silicone outgasses methane (CH_4), Fig. 2. The presence of the CMOS1 chip does not seem to affect the CO_2 and CH_4 relative partial pressure level. However, the relative amount of nitrogen (N_2) increases and argon is observable for one sample. The silicon based adhesive has better outgassing properties, but the epoxy was chosen because the CO_2 is easily pumped by the getter as compared to CH_4.[12]

Besides outgassing, other requirements have to be taken into account for the die attach process. As mentioned above the amount of epoxy should be minimized but proper thermal transfer and mechanical reliability should be achieved. A second reason for the epoxy choice is its higher shear strength. Indeed, as compared to silicone, the epoxy yields higher shear strength for the same contact surface area. The actual die surface area is approximately 1.2 cm^2. The shear strength measurement performed with a shear tester (F&K Delvotech, Austria) showed that the die can resist to a load greater than 2.5kg. This is in accordance with the MIL-STD-883G method 2019. Moreover, the adhesive area must dissipate the heat generated by the CMOS chip. Thermal transfer analysis was conducted by finite element analysis to ensure that the epoxy pattern led to a temperature uniformity within 2% over the entire bolometer active area. The parameters considered in this analysis included epoxy surface area, thermal conductance and thickness as well as electrical power to dissipate. A qualitative evaluation of proper thermal transfer is given by an infrared image. Fig. 3 shows that no unusual artifacts are observed. Also

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Table 2. Package description for adhesive IVA comparison (PG : Pressure gauges ; Base pressure : Pressure before IVA testing)

Package #	Internal components	Adhesive	Base pressure [Torr]
1	SiO_2 chip, PG	Epoxy	0.284
2	SiO_2 chip, PG	Epoxy	0.478
2	SiO_2 chip, PG	Silicone	0.052
4	CMOS1, PG	Silicone	0.026
5	CMOS1, PG	Silicone	0.0105

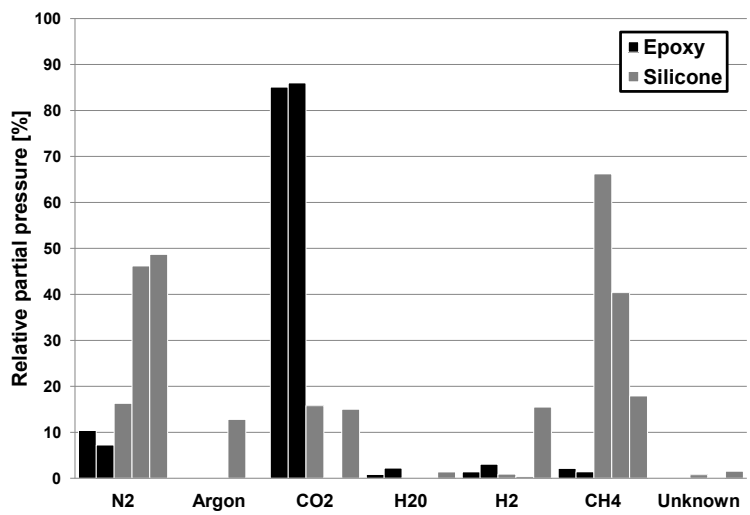

Figure 2. Comparison of IVA results for silicone and epoxy die attach adhesives. The relative partial pressure of gas species is presented. For each gas, bars from left to right represent packages number 1 to 5.

the noise equivalent temperature difference (NETD) measurements conducted at RT are comparable to those performed with an integrated TEC package technology.

Windows used for IR imaging should meet mechanical requirements related to CTE mismatch, soldering and differential pressure induced stresses. In this paper, infrared window lids made of silicon (650 μm thick) and germanium (1 mm thick) were used. These windows (20 mm squared) were directly soldered to the ceramic package. Both passed shock, vibration and temperature cycling tests as reported below.

Regarding optical requirements, the antireflection coating, AR, must have broadband transmission in the region of interest and the latter should not be affected by the getter activation temperature ($\geq$300°C). The coating should cover the clear aperture required for the focal plane array. For the CMOS1, the clear aperture area required for a F/# = 0.8 is about 10.2 x 12.2 mm. The remaining space around the clear aperture allows space for thin film non-evaporable getter deposition. The PageLid getter technology (SAES, Italy) was employed. It allows for the pumping of several active gases.

The metalization on the edge of the window matched that of the package soldering frame and was composed of a typical gold and nickel stack for fluxless soldering. The leadfree, fluxless alloy was attached to the package prior to loading it face down in the vacuum furnace equipment. The vacuum sealing equipment was a model 3150 (SST international, USA) to which a proprietary modification was added. Up to 12 packages can be simultaneously vacuum sealed. This system allows for non-evaporable getter activation on the bottom heating plate while keeping the top plate (holding temperature sensitive components) at lower temperature. The shutter

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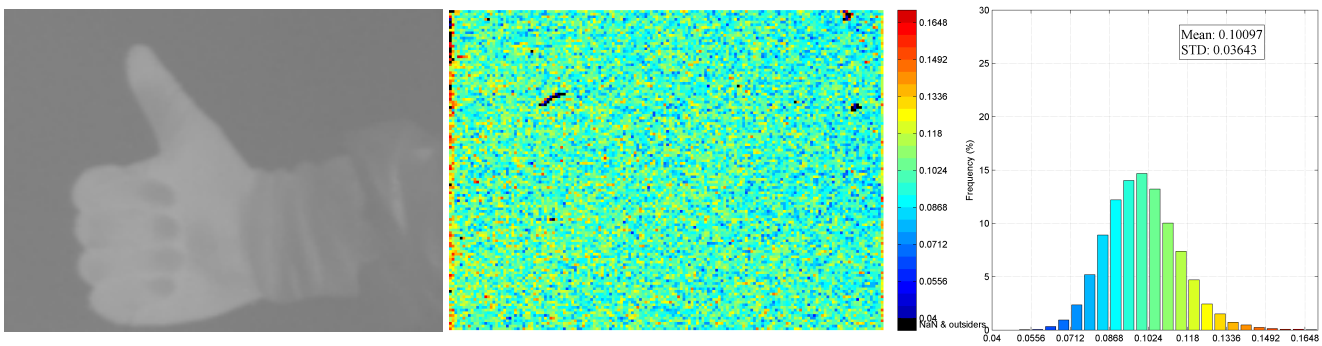

Figure 3. Infrared image obtained for 160x120 pixel FPA on CMOS1 in LCC package and external TEC (left). NETD f#/1 map (middle). Histogram of NETD value, x axis represents the NETD value in Kelvin and y axis represents the frequency of occurrence in percentage (right).

mechanism results in a temperature difference of more than a hundred degrees Celsius between the top and bottom plate. The process used in this paper includes a getter activation above 300°C while the final soldering process reaches a maximum temperature of 285°C.

2.2 Internal pressure measurement

A micro-Pirani pressure sensor was used to monitor internal cavity vacuum levels. The pressure measurement method developed by INO provides very low dependence on the substrate temperature.[13] This method is an essential tool for package pressure monitoring in that it gives precise measurement and is less time consuming than NETD measurements. As previously reported, the sensitivity limit of these devices was about 5 mTorr and the relative error increased sharply with decreasing pressure below this threshold value. In fact, the relative error was much greater than 10% below 1 mTorr. Thus, for packages exhibiting vacuum levels below this threshold, cavity pressure changes were also represented by relative changes of thermal conductivity of micro-Pirani sensors. Internal cavity pressures measured by INO microsensors and IVA were compared among 14 packages. For that purpose, the micro-Pirani was measured prior to the destructive IVA test, Fig. 4.

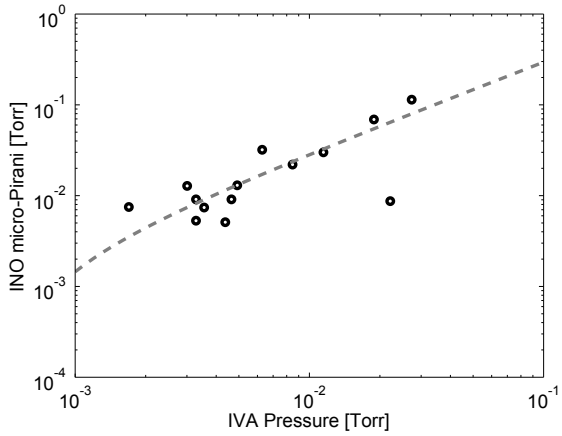

Figure 4. Correlation between the package cavity pressures measured using INO micro-Pirani pressure gauges and the IVA destructive method.

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There is a consistent difference between both measurement methods resulting in a linear slope of about 3. The results of Fig. 4 indicate that the micro-Pirani gauges overestimate the total pressure. This difference may be explained by the fact that microsensors are calibrated in air and/or that gas species present in the sealed cavity are drastically different (see section HR-IVA). The pressure determined from IVA may exhibit a large error (unknown at this point) due the lack of standard calibration packages with low pressures.

3. RESULTS

3.1 Vacuum integrity

The following section presents the systematic approach used for testing the ceramic packaging technology. The first test consisted in verifying package hermeticity. In order to determine the leak rate, the contribution of outgassing was minimized by packaging only micro-Pirani pressure gauges. The window was made of silicon and there was no AR coating. The components contributing to outgassing are the window surface, the package surface, the 2x2mm micro-Pirani silicon chip and the small amount of epoxy.

The typical pressure dependence of relative thermal conductivity changes of a micro-Pirani gauge is shown in Fig. 5a. Changes are calculated relative to the thermal conductivity value measured at a pressure of 0.5 mTorr. The measurement relative error is about 1%. This variable is presented instead of changes in base pressure since values were below the sensitivity limit of 1 mTorr. The curves of Fig. 5b demonstrate that relative changes of thermal conductance are within a few percent e.g. less than 10 mTorr after more than a year of storage at room temperature. Thus, this indicates that the sealing process provides adequate hermeticity and that there is negligible amount of outgassing.

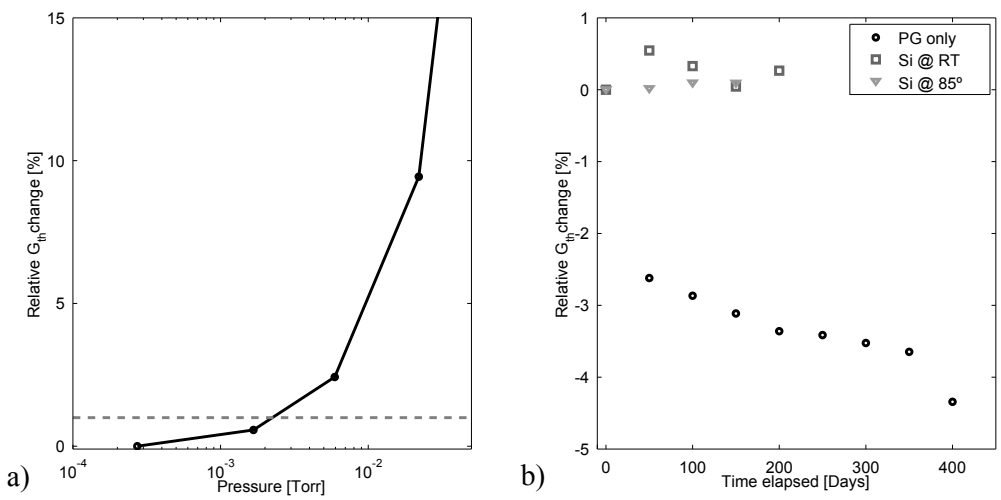

Figure 5. a) Typical pressure dependence of relative changes in thermal conductivity, G_{th}, for the micro-Pirani gauge. b) Relative change of thermal conductivity as a function of storage time for packages containing a micro-Pirani gauge only stored at RT and a bare silicon chip stored at RT and 85°C (average of 1 to 3 packages).

To evaluate the gas load related to the epoxy based die-attach process, a bare silicon chip having negligible outgassing and with dimensions similar to those of the CMOS1 FPA was then packaged. The same sealing process was applied. The lid was an AR and getter-coated germanium window. For one package with silicon chip stored at room temperature and stored at 85°C, the relative change of thermal conductivity was below 1%, Fig. 5b. Again, this is within the measurement error. This indicates that adequate amounts of epoxy do not affect the pressure inside the package even at an elevated temperature for more than 200 days.

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Finally, bolometric detectors fabricated on two types of CMOS chips were packaged. CMOS1 and CMOS2 result from fabrication processes using spin on glass and chemical mechanical polishing respectively as planarization layer. For the CMOS1 and CMOS2, the same sealing process was applied and the window was made of germanium with AR coating and getter. The base pressures obtained were always below 5 mTorr. For CMOS1, the package pressure dependence on storage time and temperature show highly variable data as illustrated by error bars, Fig. 6a. At room temperature, the pressure rose to around 20mTorr level after 100 days. At 85°C, the cavity pressure rose about 3 times as fast as compared to room temperature with significant variation in package behaviors. These results obtained for a ceramic LCC header clearly confirm those obtained for detectors fabricated on CMOS1 micropackaged in a reduced cavity volume.[4] For comparison, detectors built on CMOS2 were packaged using the same process. Five packages were assembled without any getter and six packages with getter. Due to the high uncertainty in pressure determination below 1 mTorr, relative changes of thermal conductivity are represented instead in Fig. 6b. Apart from packages stored at 120°C without getter, no significant increase of cavity pressure was observed after more than 60 days of storage at up to 120°C. Changes are within the measurement error of 1%.

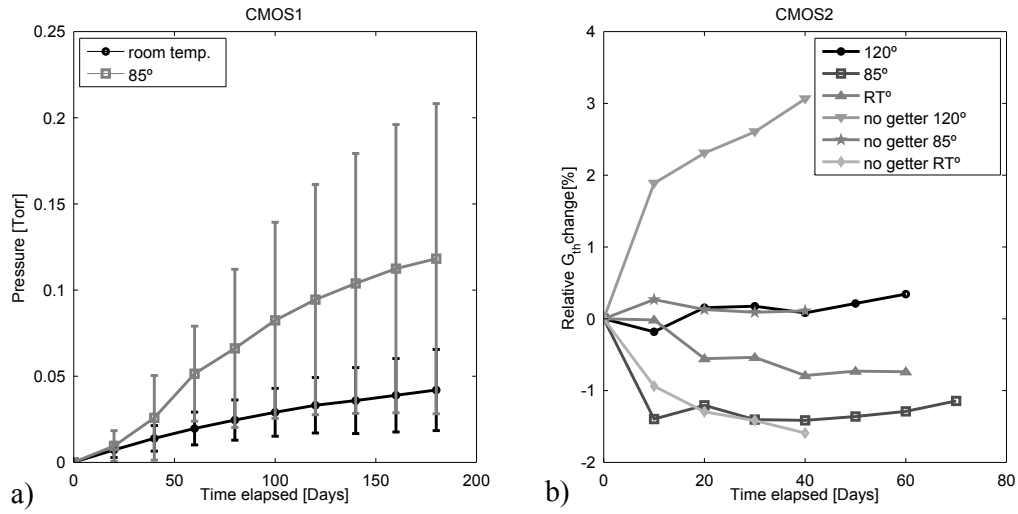

Figure 6. Package pressure and relative thermal conductivity change as a function of time for storage at various temperatures. (a) CMOS1; Mean curves of 7 packages at 85°C and 10 packages at RT are represented with error bars showing one standard deviation (1σ). b) CMOS2; Each point represents a mean value for two to three packages.

Even at a storage temperature of 85°C, thermal conductivity changes in Fig. 6b show that the pressure of packages containing CMOS2 without getter did not rise after 60 days. A similar trend was observed at room temperature.

Regarding packages with getter, those stored at 120°C exhibited the highest pressure increase as expected. It remains unclear however why packages with getter at room temperature are slightly above those stored at 85°C. Additional data is required to confirm this finding.

As can be seen in Fig. 6b, a decrease in thermal conductivity i.e. drop of pressure is observed in some cases. This may be explained by the fact that, besides the gettering effect, inner surfaces such as cavity walls are extremely clean after sealing and consequently offer reversible adsorption sites for gas molecule. Since there is not enough energy put into those molecules once adsorbed, there is no further increase of pressure over time.

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These results demonstrate that using adequate CMOS technology, mTorr pressure levels can be obtained even without getter. Such a vacuum integrity confirms adequate package design associated with proper vacuum sealing processes.

The yield was defined by the number of packages having a base pressure lower than 10 mTorr, one day after vacuum sealing. A yield over 80% was obtained for more than 10 batches containing 3 to 4 packages. Similar results were obtained for batches of up to 12 packages.

3.2 Determination of outgassed species

To account for the large pressure rise in packages containing CMOS1, high-resolution internal vapor analysis was conducted. Fourteen packages stored at different accelerating temperatures, 22°C, 60°C, 75°C and 85°C for a period of time varying from 40 to 60 days, were analyzed. The histogram of all the packages shows a similar gas composition, Fig. 7. The main species that composed the gas load were argon and methane with median levels of 53% and 42% respectively. It was found that the relative partial pressure of a given gas species did not depend on the storage temperature.

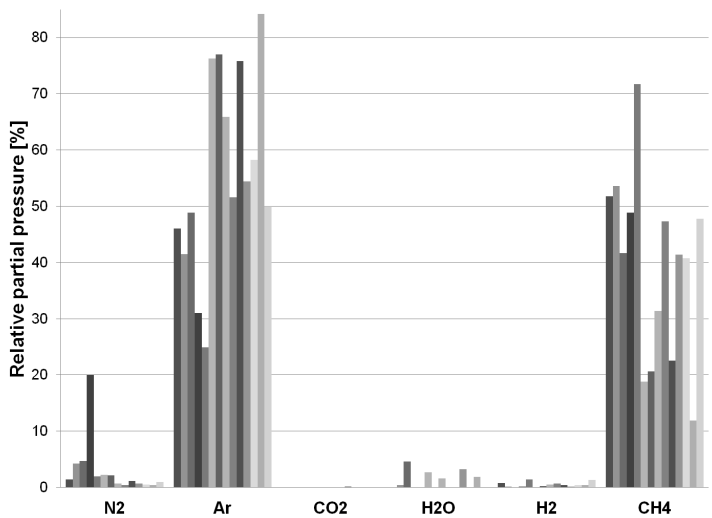

Figure 7. Gas composition of 14 packages subjected to IVA. The relative partial pressure of main gases is presented. For a given gas, each bar corresponds to a package.

The absolute partial pressures represented in Fig. 8 reveal that in most cases active gases such as CO_2, H_2O and H_2 are kept at low levels, even for high package pressure. This confirms that the getter is pumping and also that no significant leaks are present. The partial pressure of argon and methane increases with increasing package pressure. The presence of N_2 in a package having a pressure above 25 mTorr most likely indicates a leak. Nevertheless, the source of methane is not fully understood at this time and is clearly a major contributor to the degradation of vacuum in packages containing CMOS1.

Previous work conducted on a non evaporable getter, ST707 from SAES, showed that the CH_4 presence and evolution resulted from a reaction between adsorbed carbon dioxide and hydrogen.[14] The getter alloy employed in this study (PaGeLid ST787 from SAES) has similarities with the ST707 alloy in that they are both mainly composed of zirconium. The PageLid getter absorbs both CO_2 and H_2. The IVA data of Fig. 7 confirms that the level of CO_2 and H_2 is low among the 14 packages. It is suggested that both gases react to produce methane, which exhibits an increasing partial pressure with storage time. The IVA analysis of Fig. 2 showed that CMOS1

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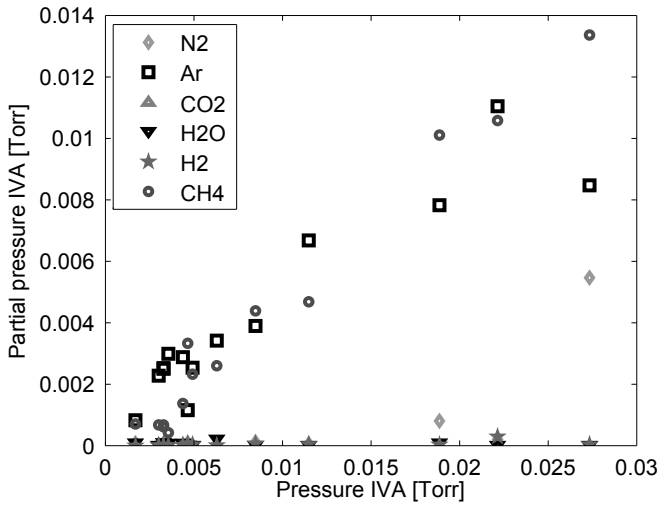

Figure 8. Absolute partial pressure versus total package pressure, both measured by IVA for various gases.

produced limited amounts of CO_2 when combined with a silicone based die-attach. On the other hand, the epoxy die-attach released large proportions of CO_2, Fig. 2. One solution towards reduction of the CH_4 production for the packaging of CMOS1 may be to reduce the CO_2 level adsorbed by replacing the epoxy die attach by a soldering process.

3.3 Reliability

The reliability of vacuum sealed packages with regards to standard environmental stresses was investigated. Two packages containing bolometric detectors fabricated on CMOS1 were submitted consecutively to the tests described in table 3. Vacuum performance of packages was measured using pressure microsensors and by the signal transfer function (SiTF) of the FPA. The SiTF depends on the dectector responsivity and is expressed in output counts per changes of scene temperature. For each test, the hermeticity was preserved since no pressure increase was observed in the cavity. In fact, changes in cavity pressure over the duration of the test campaign seen in Fig. 9a are comparable to those previously shown (Fig. 6a) for storage of 25 days at room temperature, e.g. 0.2 mTorr per day. Moreover, the SiTF measurement did not show any degradation since measured variations were within the measurement error (e.g. relative SiTF error of 5%) Fig. 9b. Note also that the pressure rise over the period did not have a noticeable effect on SiTF.

Table 3. Description of environmental tests.

Test	Standard	Method	Description
Vibration	MIL-STD-810	514	0.06 g/Hz from 10Hz-2kHz perpendicular and parallel axis of FPA. 10.9 g RMS 1 hour per axis.
Shock	MIL-STD-810	516	20 g, 10 ms, perpendicular and parallel axis of FPA, 2 shocks per axis.
Thermal cycling	MIL-STD-810	501	30 cycles, -55 °C to 85°C, ramp 20 min and soak 20 min.
Temperature/Humidity	GR-1209-CORE	—	85°C @ 85% humidity during 100 hours

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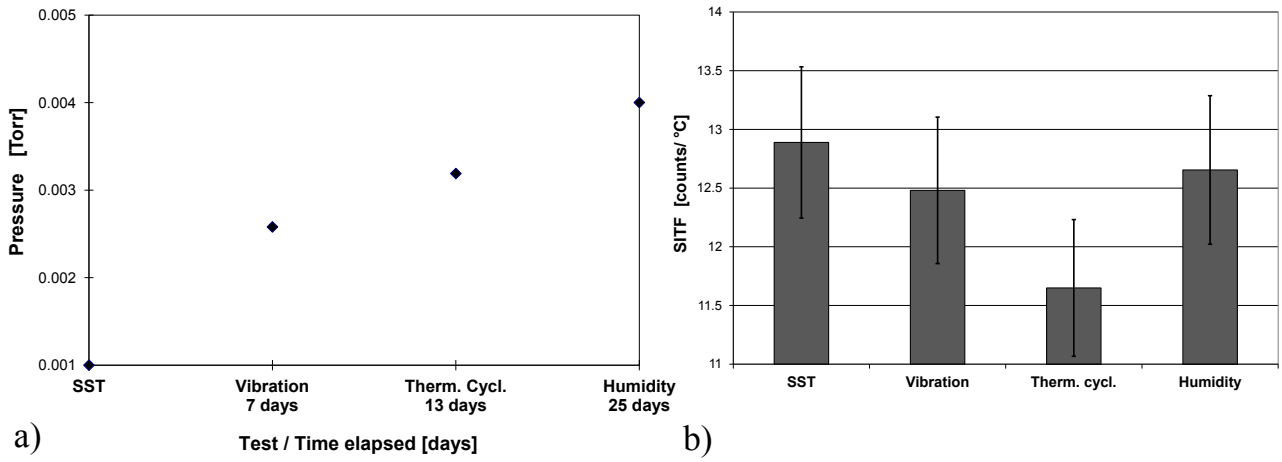

Figure 9. a) Cavity pressure measured after each reliability test of table 3. b) Signal transfer function (SiTF) after each test. The bar SST represents the value measured a few hours after vacuum sealing.

3.4 Lifetime

To compare the lifetime of CMOS1 and CMOS2 at room temperature, an equivalent leak rate was calculated assuming an activation energy of 12 Kcal/mol.[12] Curves for accelerated aging at RT for CMOS1 and 120°C for CMOS2 with and without getter were fitted with a simple linear model. This represents a worst case since more refined models[4] must take saturation effects into account. To determine leak rates at RT, an acceleration factor of 164 was calculated assuming an Arrhenius dependence[15] using an activation energy of 0.52 eV. The equivalent leak rate at RT for packages containing CMOS1 was 8.2×10^{-13} Torr*L/sec whereas that of packages containing CMOS2 was 9.1×10^{-17} Torr*L/sec. If we assume a failure criterion of 1.5 times the initial NETD value, this corresponds to a 50 mTorr pressure increase as measured for packages CMOS1 FPAs. Thus, in this case, the lifetime calculated using the model[4] and acceleration factor of 164 gives 219 days for CMOS1 and well above ten years for CMOS2.

4. CONCLUSION

In this paper, a TECless ceramic vacuum packaging technology for uncooled bolometric FPAs was described. To avoid potential damage of components, INOs packaging technology uses a maximum process temperature of 285°C. The process is however compatible with AuSn as solder material provided CMOS chips can withstand associated reflow profiles. Results demonstrate that optimized assembly and vacuum sealing processes can yield packages with the required vacuum integrity even using thermally conductive epoxy as die-attach material. Base pressures below 3 mTorr were obtained. Negligible cavity pressure changes were achieved even for packages without getter stored for more than 60 days at up to 85°C. When a getter thin film was applied on the window, equivalent leak rates of the order of 10^{-16} Torr*L/s were calculated at room temperature. Results clearly demonstrate that CMOS circuits can be the dominant contributor to outgassing. For one of the CMOS circuits studied, significant partial pressures of argon and methane were evident from internal vapor analysis, explaining the significant pressure rise with time. The packaging technology complies with standard MIL-STD-810 environmental tests. Packaging yields over 80% were obtained.

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ACKNOWLEDGMENTS

We wish to thank Heather Florence from SAES getter group and Daniel Rossiter from Oneida Research Services, inc. for helpful discussions.

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